**Amendment to the Abstract:**

Pease cancel the previous abstract and replace it with the following abstract:

A CRC circuit, CRC method, and method of designing a CRC circuit, the CRC circuit, including: a packet data slice latch having outputs; a multiple level XOR subtree, each level including one or more XOR subtrees, each output of the packet data slice latch coupled to an input of the multiple level XOR subtree, each lower level XOR subtree coupled to a higher level XOR subtree through an intervening latch level; a remainder XOR subtree; a combinational XOR subtree, the outputs of the remainder XOR subtree and the outputs of the multiple level XOR subtree coupled to the inputs of the combinational XOR subtree; and a current CRC result latch, the output of the combinational XOR subtree coupled to the inputs of the current CRC result latch and the outputs of the M-bit current CRC result latch coupled to the inputs of the remainder XOR subtree.